Amendments to the Specification:

Please replace the paragraph beginning on page 9, line 20 and continuing to page 10, line 9 of the Specification with the following replacement paragraph which has been marked up to show the changes to the paragraph.

The overlap regions 58 are turned on during the reset cycle. The overlap regions 58 are then turned [[on]] <u>off</u> during the charge integration period. After the completion of the charge integration period the overlap regions 58 can be used to control the charge transfer from the deep N well 56 to each of the N wells 52. The pixel is read by reading the potential of the N wells 56. In one mode of operation the potential of the N wells 56 can be read before and after the transfer of the charge from the deep N well 56 to each N well 56 providing a pixel correlated double sampling operation. The first 51 and second 53 N regions in each of the P wells 50 provide electrical communication to each of the P wells 50. The P region in each of the N wells 52 provide electrical communication to each of the N wells 52. The first N region 51, second N region 53, and P well 50 in each N well 52 can be used as a floating gate field effect transistor. In this structure P well regions 50 formed in each of the N wells 52 can be used as a floating gate sense node for alternative non-destructive readout.